AMENDMENTS TO THE CLAIMS

Listing of claims:

This listing of claims replaces all prior versions and listings of claims in the application.

1. (currently amended) A semiconductor storage device comprising:

a memory cell transistor having a first diffused layer and a second diffused layer formed in a semiconductor substrate, and a gate electrode formed over the semiconductor substrate between the first diffused layer and the second diffused layer with a gate insulation film interposd therebetween;

an insulation film covering a top of the memory cell transistor and having a through-hole opened on the first diffused layer and an opening surrounding the through-hole, the opening having a larger diameter than the through-hole and not reaching the semiconductor substrate;

a capacitor storage electrode formed on an inside wall and a bottom of the opening and electrically connected to the first diffused layer, a thickness of the capacitor storage electrode being thinner than a depth of the opening;

a capacitor dielectric film formed covering the capacitor storage electrode; and

a capacitor opposed electrode formed coving the capacitor dielectric film.

2. (original) A semiconductor storage device according to claim 1, wherein the capacitor storage electrode includes a columnar conductor buried in the through-hole and projected in the opening.

3. (original) A semiconductor storage device according to claim 1, wherein the insulation film is formed in a laminated film of two or more films laid one on another, and the adjacent films have different etching characteristics from each other.

4. (currently amended) A semiconductor storage device ~~according to claims 1, wherein~~ comprising:

a memory cell transistor having a first diffused layer and a second diffused layer formed in a semiconductor substrate, and a gate electrode formed over the semiconductor substrate between the first diffused layer and the second diffused layer with a gate insulation film interposed therebetween;

an insulation film covering a top of the memory cell transistor and having a through-hole opened on the first diffused layer and an opening surrounding the through-hole, the opening having a larger diameter than the through-hole and not reaching the semiconductor substrate;

a capacitor storage electrode formed on an inside wall and a bottom of the opening and electrically connected to the first diffused layer, the opening ~~is~~ being not fully filled with the capacitor storage electrode.

5. (canceled)

6. (previously presented) A semiconductor storage device according to claim 1, wherein the capacitor storage electrode is formed along the inside wall and the bottom of the opening.